# **Power MOSFET**

# 80 V, 9.5 m $\Omega$ , 68 A, Single N-Channel

#### **Features**

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

#### **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	80	V
Gate-to-Source Voltage	e		$V_{GS}$	±20	V
Continuous Drain		$T_C = 25^{\circ}C$	I <sub>D</sub>	68	Α
Current R <sub>θJC</sub> (Notes 1, 2, 3, 4)	Steady State	T <sub>C</sub> = 100°C		48	
Power Dissipation		T <sub>C</sub> = 25°C	P <sub>D</sub>	107	W
R <sub>θJC</sub> (Notes 1, 2, 3)		T <sub>C</sub> = 100°C		53	
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	11	Α
Current R <sub>θJA</sub> (Notes 1 & 3, 4)	Steady State	T <sub>A</sub> = 100°C		8.4	
Power Dissipation		T <sub>A</sub> = 25°C	$P_{D}$	3.2	W
R <sub>θJA</sub> (Notes 1, 3)		T <sub>A</sub> = 100°C		1.6	
Pulsed Drain Current $T_A = 25^{\circ}C$ , $t_p = 10 \mu s$			I <sub>DM</sub>	300	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	ç
Source Current (Body Diode)			IS	89	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L(pk)</sub> = 3.4 A)			E <sub>AS</sub>	271	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 3)	$R_{\theta JC}$	1.4	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{\theta JA}$	47	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Psi  $(\Psi)$  is used as required per JESD51–12 for packages in which substantially less than 100% of the heat flows to single case surface.
- 3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

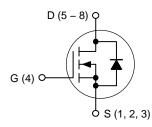


## ON Semiconductor®

#### www.onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
80 V	9.5 mΩ @ 10 V	68 A

#### N-Channel



# MARKING DIAGRAM

# WDFN8 (μ8FL) CASE 511AB



850N = Specific Device Code A = Assembly Location

Y = Year WW = Work Week • Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

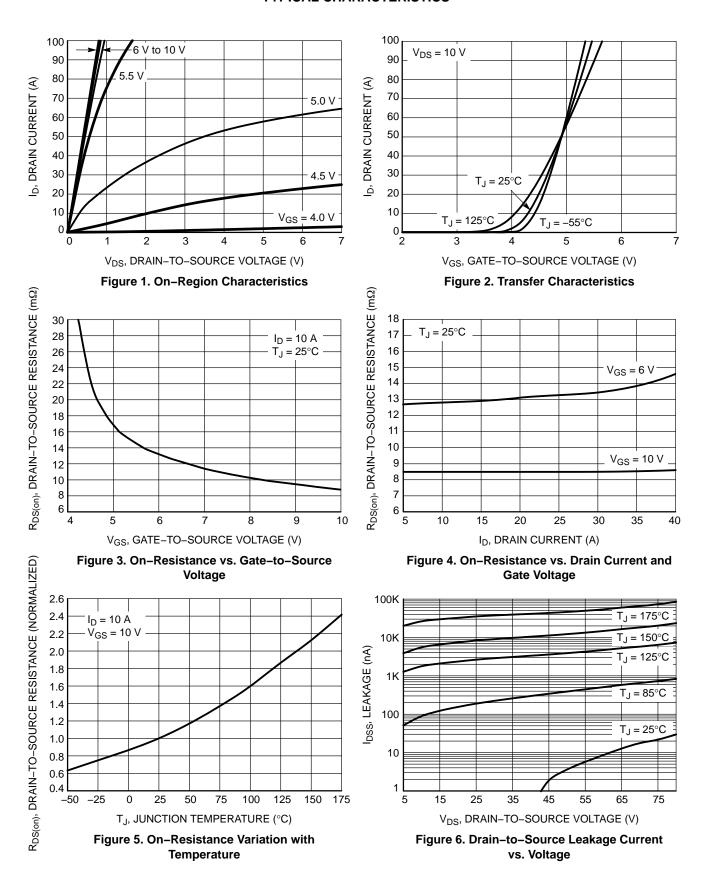
See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		80			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{CS} = 0 \text{ V}$ $T_{J} = 25^{\circ}\text{C}$				10	μΑ
		$V_{GS} = 0 \text{ V}, V_{DS} = 80 \text{ V}$	T <sub>J</sub> = 125°C			250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS}$	<sub>S</sub> = 20 V			100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D}$	= 70 μΑ	2.0		4.0	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>E</sub>	) = 10 A		8.5	9.5	mΩ
		$V_{GS} = 6 \text{ V}, I_D$	= 10 A		13	17	
Forward Transconductance	9 <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>E</sub>	) = 10 A		63		S
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>iss</sub>				1140		pF
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V, f} = 0$	1.0 MHz,		175		
Reverse Transfer Capacitance	C <sub>rss</sub>	$V_{DS} = 40 \text{ V}$			10		
Output Charge	Q <sub>oss</sub>	1			25		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				3.6		nC
Gate-to-Source Charge	$Q_{GS}$	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 40 V, I <sub>D</sub> = 10 A			6.5		
Gate-to-Drain Charge	$Q_{GD}$	1			3.7		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10 \text{ V}, V_{DS} = 4$	0 V, I <sub>D</sub> = 10 A		19		nC
SWITCHING CHARACTERISTICS (No	te 6)						
Turn-On Delay Time	t <sub>d(on)</sub>				11		ns
Rise Time	t <sub>r</sub>	$V_{GS} = 6.0 \text{ V}, V_{D}$	s = 64 V,		32		
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS} = 6.0 \text{ V}, V_{DS} = 64 \text{ V},$ $I_{D} = 10 \text{ A}$			34		
Fall Time	t <sub>f</sub>				8.0		
DRAIN-SOURCE DIODE CHARACTER	RISTICS						
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.8	1.2	V
		$I_{S} = 10 \text{ A}$ $T_{J} = 125^{\circ}\text{C}$			0.7		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } dl_S/dt = 100 \text{ A/}\mu\text{s,}$ $l_S = 10 \text{ A}$			40		ns
Charge Time	t <sub>a</sub>				24		
Discharge Time	t <sub>b</sub>				16		
Reverse Recovery Charge	Q <sub>RR</sub>				40		nC

<sup>5.</sup> Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



#### TYPICAL CHARACTERISTICS

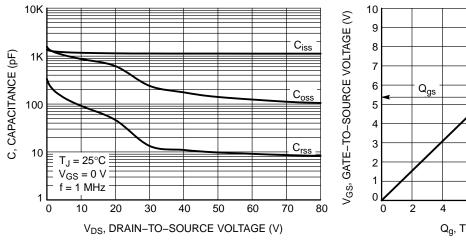


Figure 7. Capacitance Variation

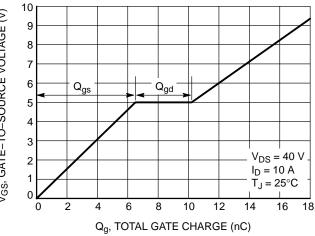


Figure 8. Gate-to-Source vs. Total Charge

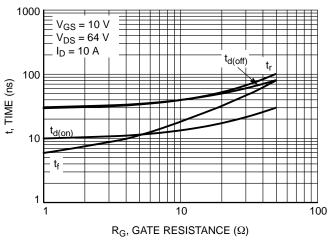


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

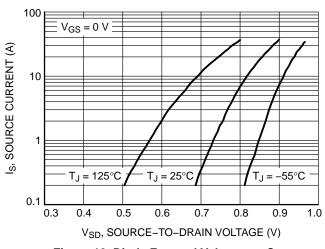


Figure 10. Diode Forward Voltage vs. Current

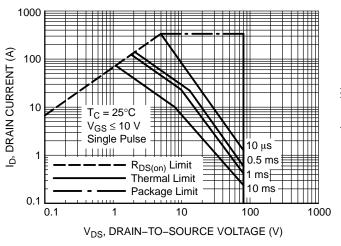


Figure 11. Maximum Rated Forward Biased Safe Operating Area

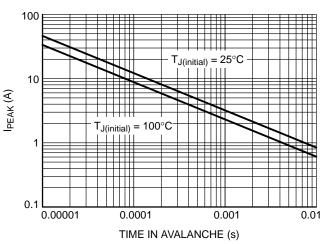


Figure 12. Maximum Drain Current vs. Time in Avalanche

### **TYPICAL CHARACTERISTICS**

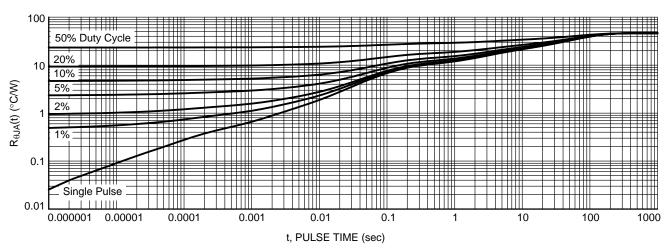


Figure 13. Thermal Response

## **DEVICE ORDERING INFORMATION**

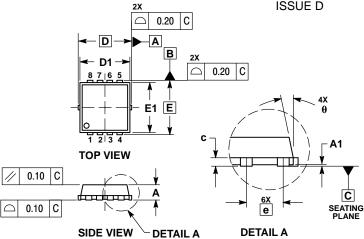
Device	Marking	Package	Shipping <sup>†</sup>	
NTTFS6H850NTAG	850N	WDFN8 (Pb-Free)	1500 / Tape & Reel	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

## WDFN8 3.3x3.3, 0.65P

CASE 511AB ISSUE D

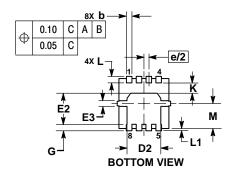


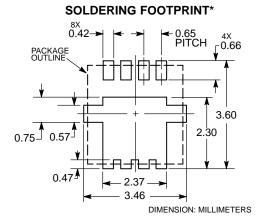
#### NOTES:

- OTES.

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS				INCHES	
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
С	0.15	0.20	0.25	0.006	0.008	0.010
D		3.30 BSC		0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
Е	3.30 BSC			C	.130 BSC	
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
е	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	800.0
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °		12 °	0 °		12 °





\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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