International IOR Rectifier

IRDC3823-P1V2

SupIRBuck™

USER GUIDE FOR IRDC3823 EVALUATION BOARD

1.2Vout

DESCRIPTION

The IR3823 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 3.5mm X 3.5 mm Power QFN package.

Key features offered by the IR3823 include selectable Digital Soft Start, precision 0.6Vreference voltage, Power Good, thermal protection, programmable switching frequency, Enable input, input under-voltage lockout for proper start-up, enhanced line/ load regulation with feed forward, external frequency synchronization with smooth clocking, internal LDO and pre-bias start-up.

Output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous MOSFET for optimum cost and performance and the current limit is thermally compensated.

This user guide contains the schematic and bill of materials for the IRDC3823 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3823 is available in the IR3823 data sheet.

BOARD FEATURES

- V_{in} = +12V (+ 13.2V Max)
- V_{out} = +1.2V @ 0- 3A
- F_s=1000kHz
- L= 1.0uH (4.0mm X 4.0mm X 2.1mm, DCR=10.8mΩ)
- C_{in}= 2x10uF (25V, ceramic 1206) + 1X100uF (25V, electrolytic)
- C_{out}=1x22uF (6.3V, ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum of 3A load should be connected to VOUT+ and VOUT-. The inputs and output connections of the board are listed in Table I.

IR3823 has only one input supply and internal LDO generates Vcc from Vin. If operation with an external Vcc is required, remove R7 and solder a zero ohm resistor for R5. Then an external Vcc can be applied between Vcc+ and Vcc- pins. Vin pin and Vcc/LDO_Out pins should be shorted together for the external Vcc operation.

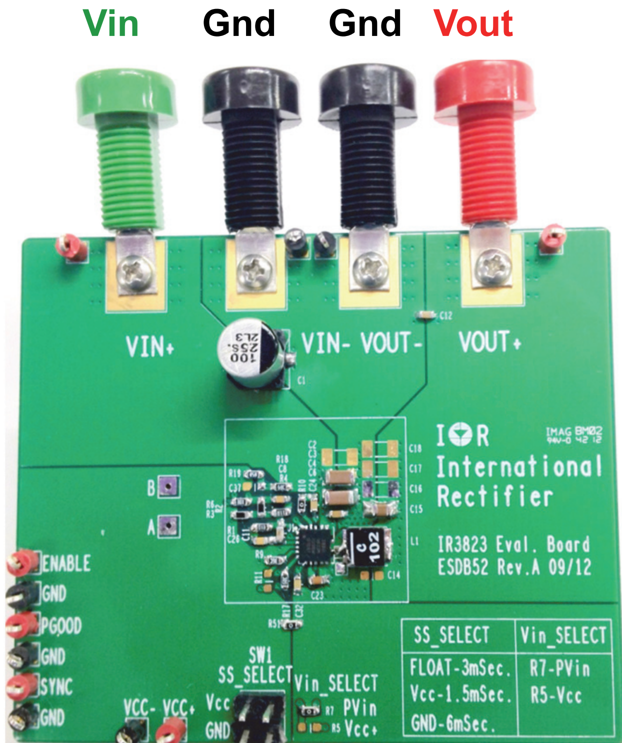
Table I. Connections

Connection	Signal Name
VIN+	Vin (+12V)
VIN-	Ground of Vin
Vout+	Vout(+1.2V)
Vout-	Ground for Vout
Vcc+	Vcc/ LDO_Out Pin
Vcc-	Ground for Vcc input
Enable	Enable
PGood	Power Good Signal
Sync	Synchronization
Gnd	Analog ground
SS_Select (Soft-start Selection)	Vcc: SS time = 1.5m sec
	Float: SS time = 3m sec
	Gnd: SS time = 6 m sec

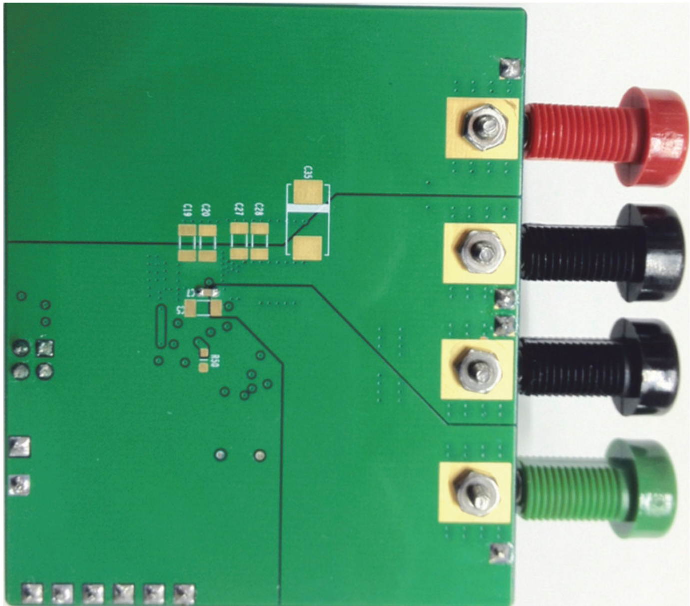
LAYOUT

The PCB is a 2.6"x 2.2" 4-layer board using FR4 material. All layers use 2 Oz. copper. The PCB thickness is 0.062". The IR3823 and other major power components are mounted on the top side of the board. Power supply decoupling capacitors, the bootstrap capacitor and feedback components are located close to IR3823. The feedback resistors are connected to the output at the point of regulation and are located close to the SupIRBuck IC. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

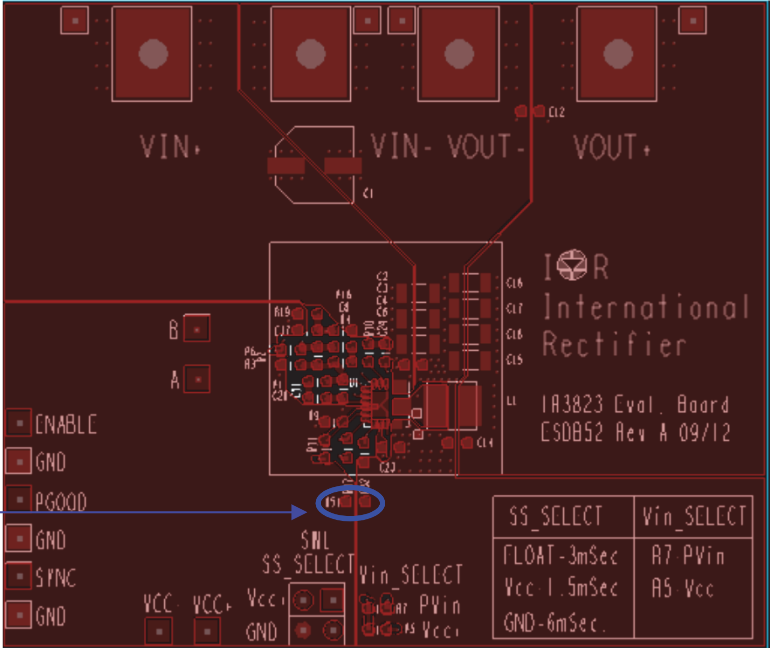


Top View



Bottom View

Fig. 1: Connection Diagram of IR3823 Evaluation Boards



Single point connection between AGnd and PGnd

Fig. 2: Board Layout-Top Layer

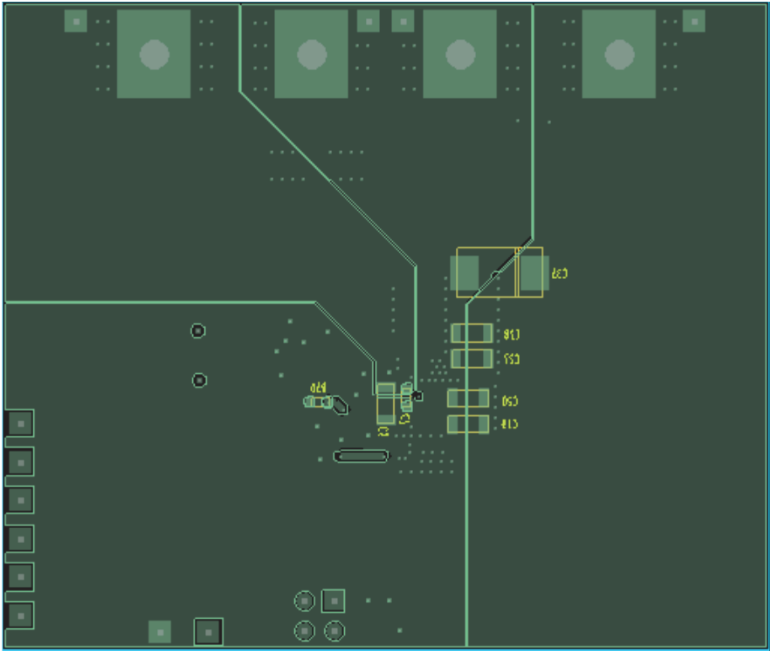


Fig. 3: Board Layout-Bottom Layer

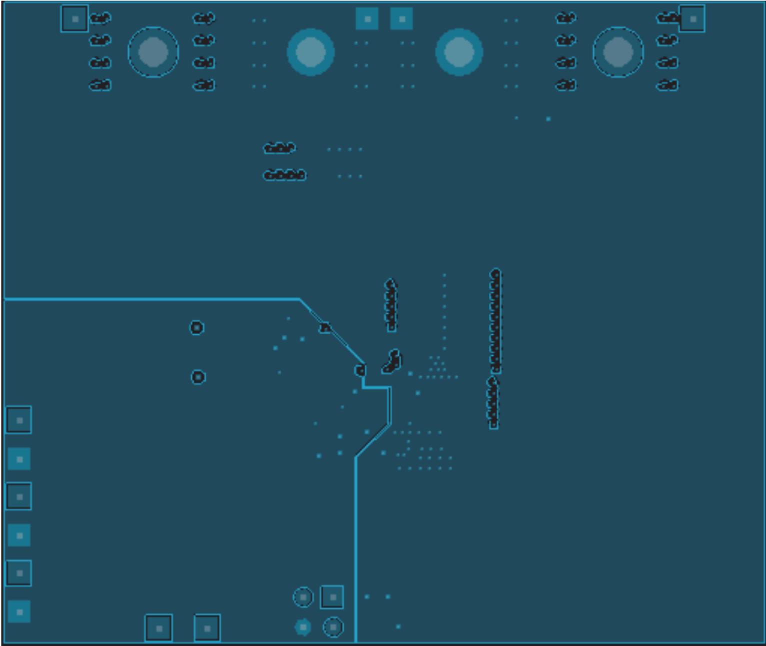


Fig. 4: Board Layout-Mid Layer 1

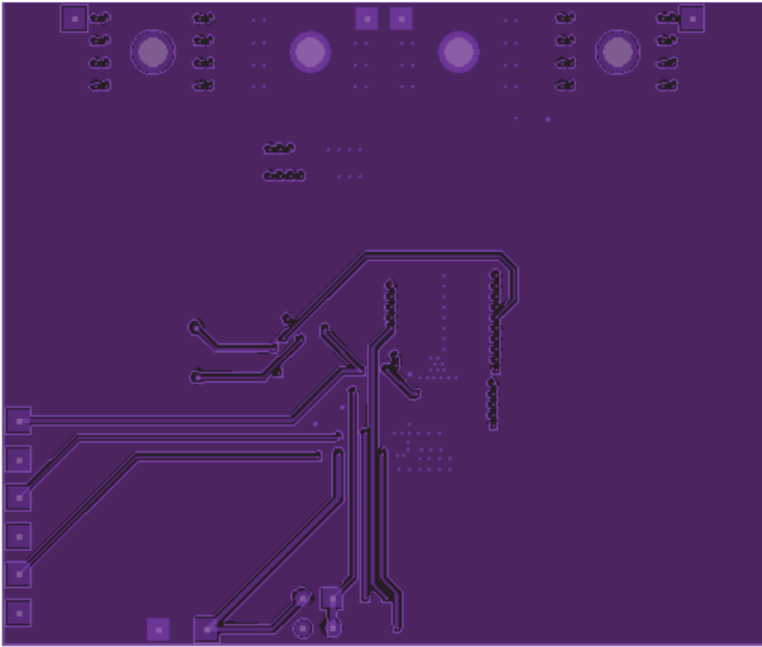


Fig. 5: Board Layout-Mid Layer 2

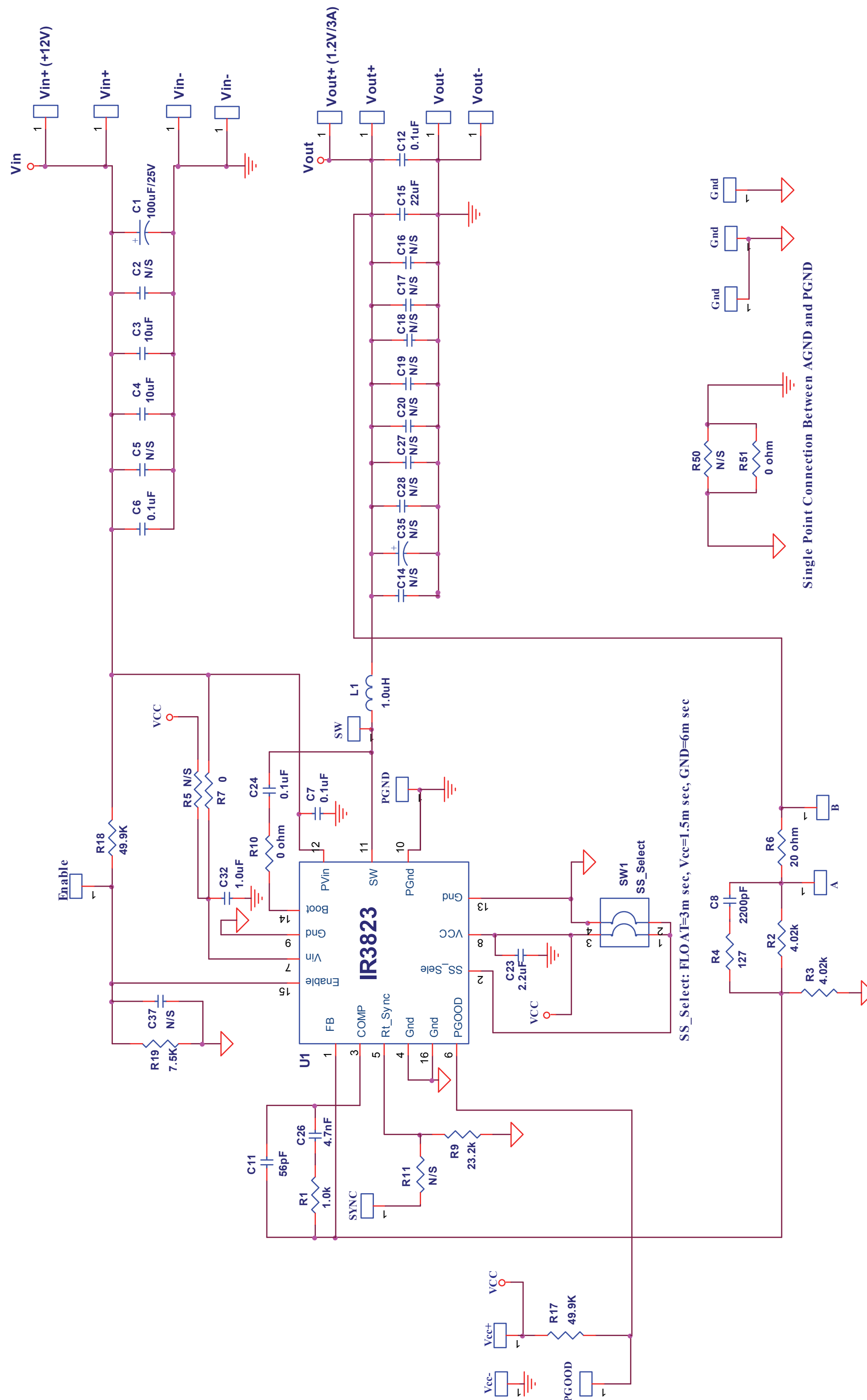


Fig. 6: Schematic of the IRDC3823 evaluation board Vin=12V, Vo=1.2V, Iomax=3A

Bill of Materials

Item	Qty	Part Reference	Value	Description	Manufacturer	Part Number
1	1	C1	100uF	CAP ALUM 100UF 25V 20% SMD	Panasonic	EEE-1EA101XP
2	2	C3, C4	10uF	1206, 25V, X5R, 20%	TDK	C3216X5R1E106M
3	4	C6, C7, C12, C24	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01B
4	1	C11	56pF	0603, 50V, NP0, 5%	TDK	C1608C0G1H560J080AA
5	1	C15	22uF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J226M
6	1	C8	2200pF	0603,50V,X7R	Murata	GRM188R71H222KA01B
7	1	C23	2.2uF	0603, 16V, X5R, 20%	TDK	C1608X5R1C225M
8	1	C26	4700pF	0603, 50V 10% X7R	Murata	GRM188R71H472KA01D
9	1	C32	1.0uF	0603, 25V, X5R, 10%	Murata	GRM188R61E105KA12D
10	1	R1	1.0k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1001V
11	2	R2, R3	4.02k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4021V
12	1	R4	127	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1270V
13	1	R6	20	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF20R0V
14	3	R7, R10, R51	0	Thick Film, 0603,1/10W	Panasonic	ERJ-3GEY0R00V
15	1	R9	23.2k	Thick Film, 0603,1/10W	Panasonic	ERJ-3EKF2322V
16	2	R17, R18	49.9k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4992V
17	1	R19	7.5k	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF7501V
18	1	L	1.0uH	SMD, 4.0mmx4.0mmx2.1mm, 10.8mΩ	Coilcraft	XFL4020-102
19	1	U1	IR3823	3A POL, PQFN 3.5mm x3.5mm	IR	IR3823

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vo=1.2V, Io=0-4A, Room Temperature, no airflow

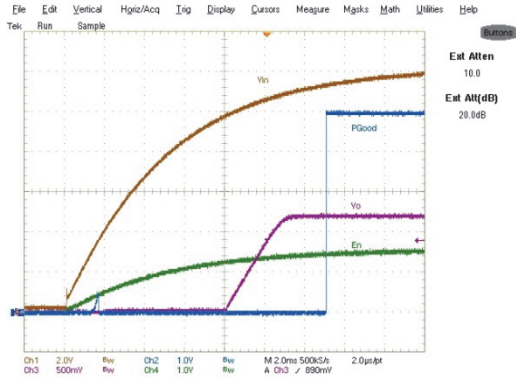


Fig. 7: Start up at 3A Load with SS_Select pin floating Ch_1:V_{in}, Ch_2:P_{Good}, Ch_3:V_o ,Ch_4:Enable

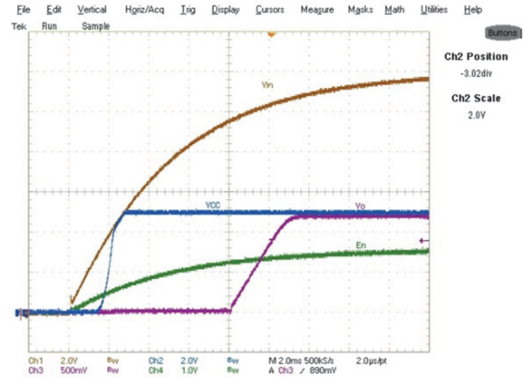


Fig. 8: Start up at 3A Load with SS_Select pin floating Ch_1:V_{in}, Ch_2:V_{cc}, Ch_3:V_o ,Ch_4:Enable

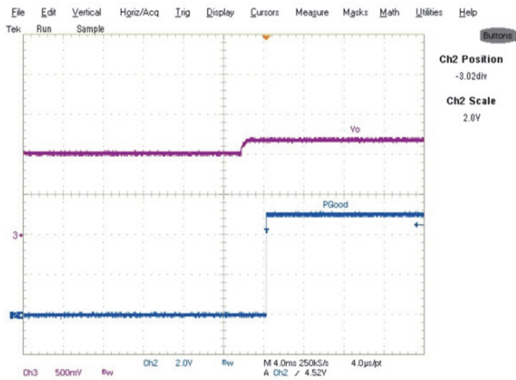


Fig. 9: Start up with 1V Pre Bias , 0A Load, Ch_2:P_{Good}, Ch_3:V_o

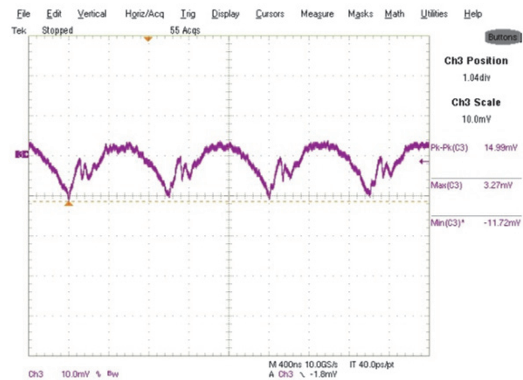


Fig. 10: Output Voltage Ripple, 3A load Ch_2: V_{out} ,

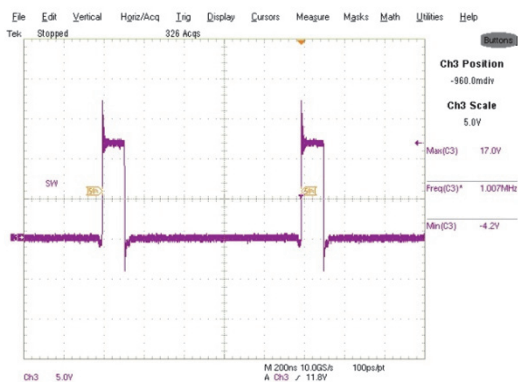


Fig. 11: Inductor node at 3A load Ch_3:LX

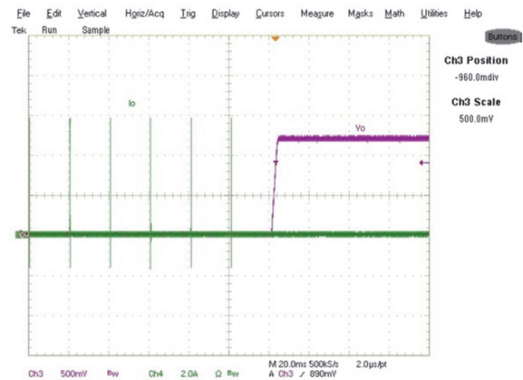
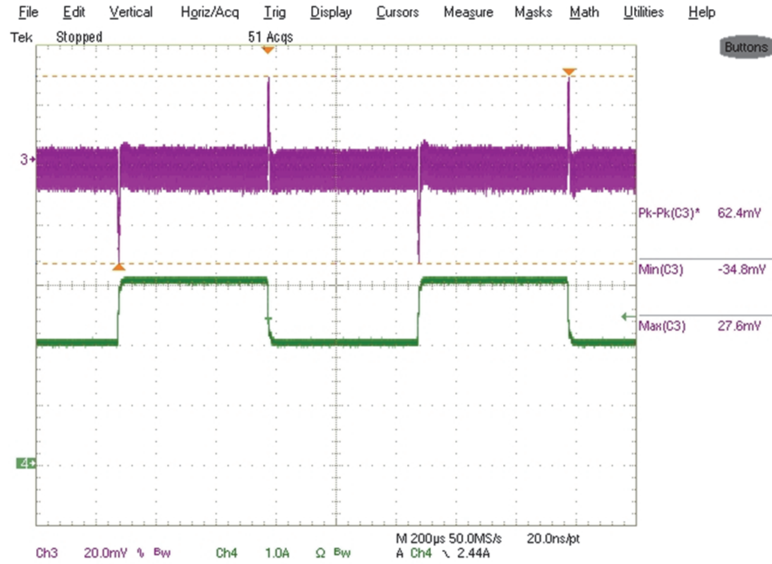
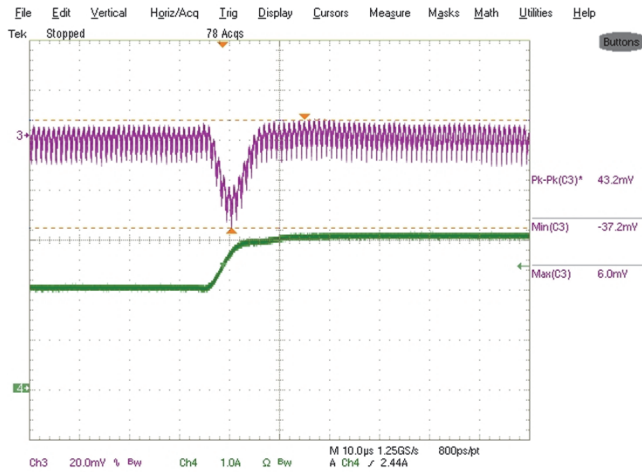


Fig. 12: Short circuit (Hiccup) Recovery, with SS_Select pin floating, Ch_3:V_{out} , Ch4:Iout

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vo=1.2V, Io=0-3A, Room Temperature, no air flow





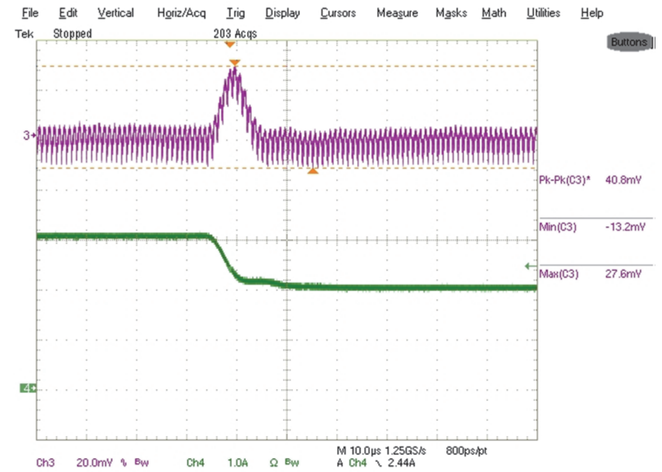
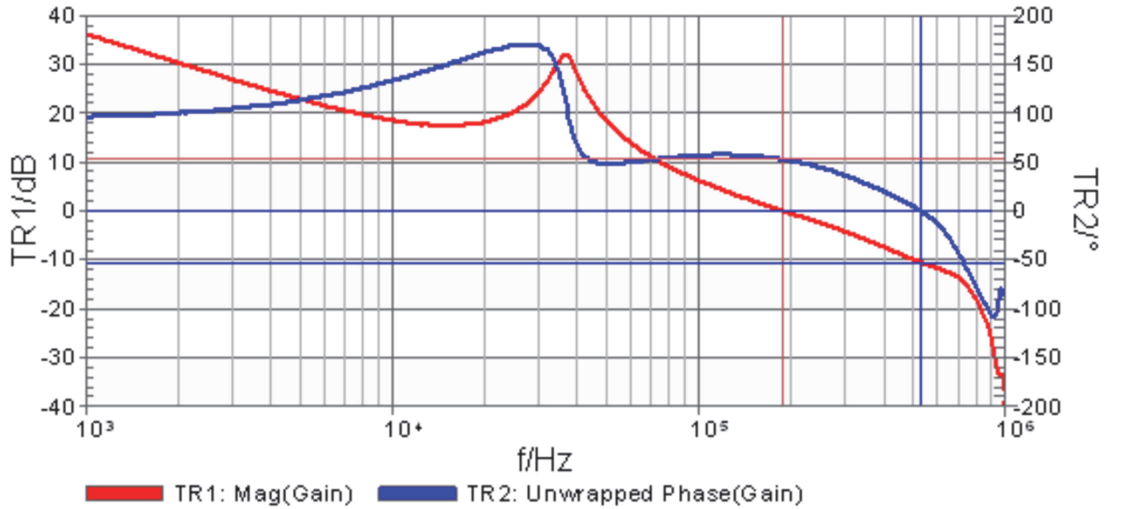


Fig. 13: Transient Response, 2.0A to 3A step
Ch_2:V_{out} Ch4-I_{out}

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vo=1.2V, Io=0-3A, Room Temperature, no air flow



	Frequency	Trace1		Trace2	
Cursor 1	188.366 kHz		0.000 dB		52.895 °
Cursor 2	528.174 kHz		-10.478 dB		-227.374 f°

Fig. 14: Bode Plot at 3A load shows a bandwidth of 188kHz and phase margin of 53 degrees and gain margin of -10dB

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vo=1.2V, Io=0-3A, Room Temperature, no air flow

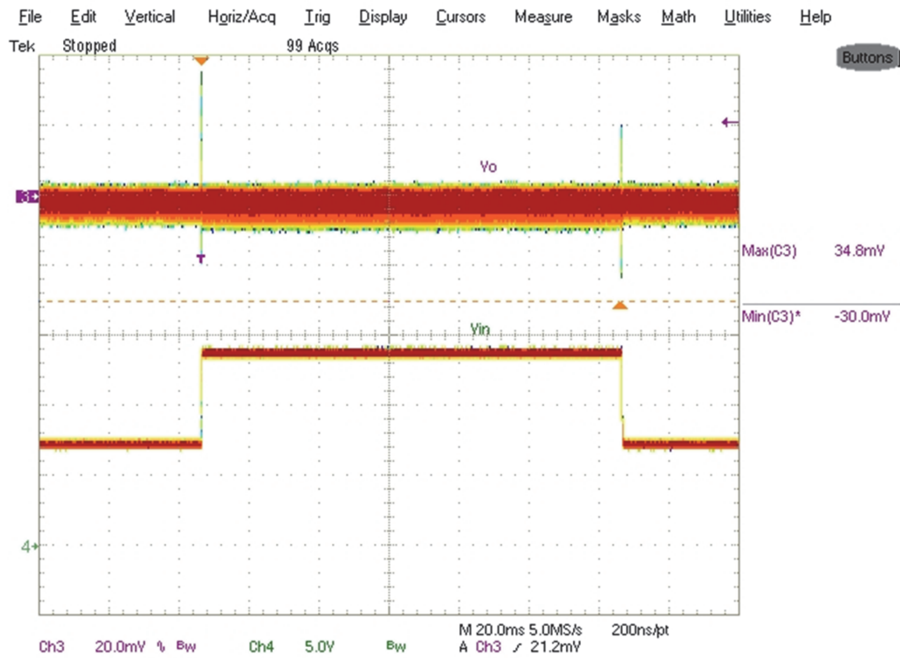


Fig 15. Feed Forward for Vin change from 7 to 14V and back to 7V
Ch_3-Vout Ch_4-Vin

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vo=1.2V, Io=0-3A, Room Temperature, no air flow

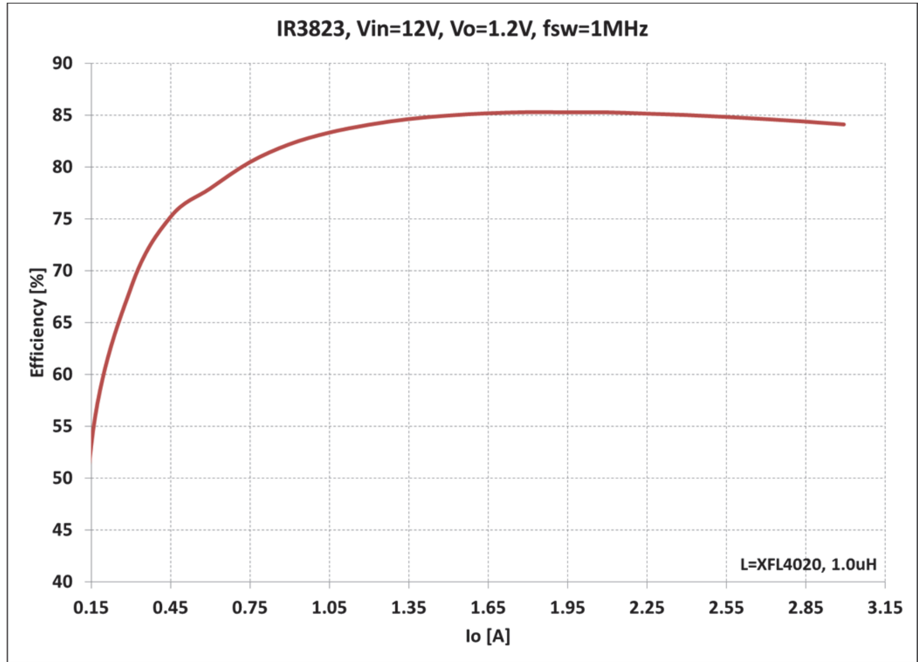


Fig.16 : Efficiency versus load current

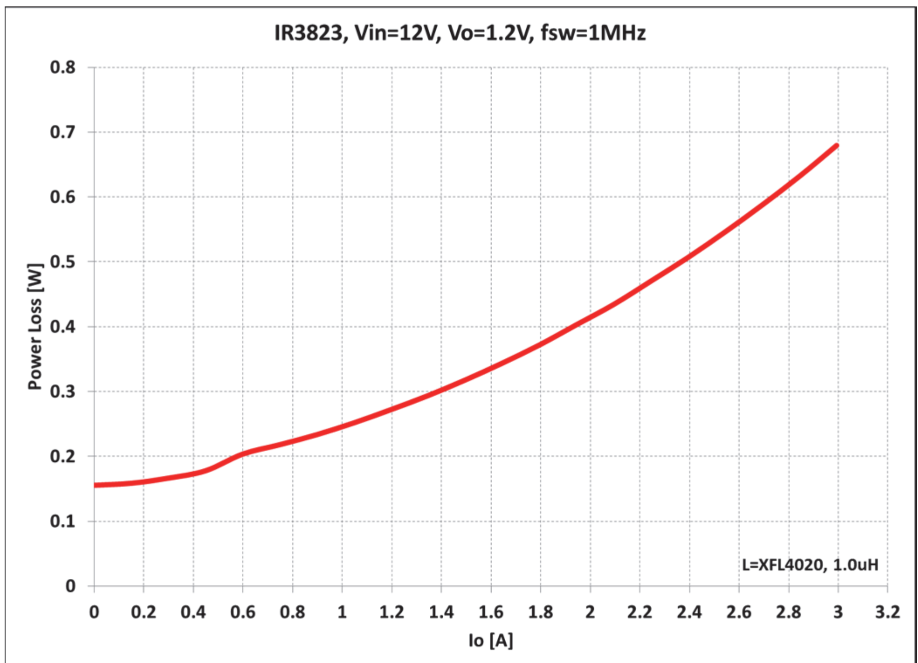


Fig.17: Power loss versus load current

THERMAL IMAGES
Vin=12.0V, Vo=1.2V, Io=3A, Room Temperature, No Air flow

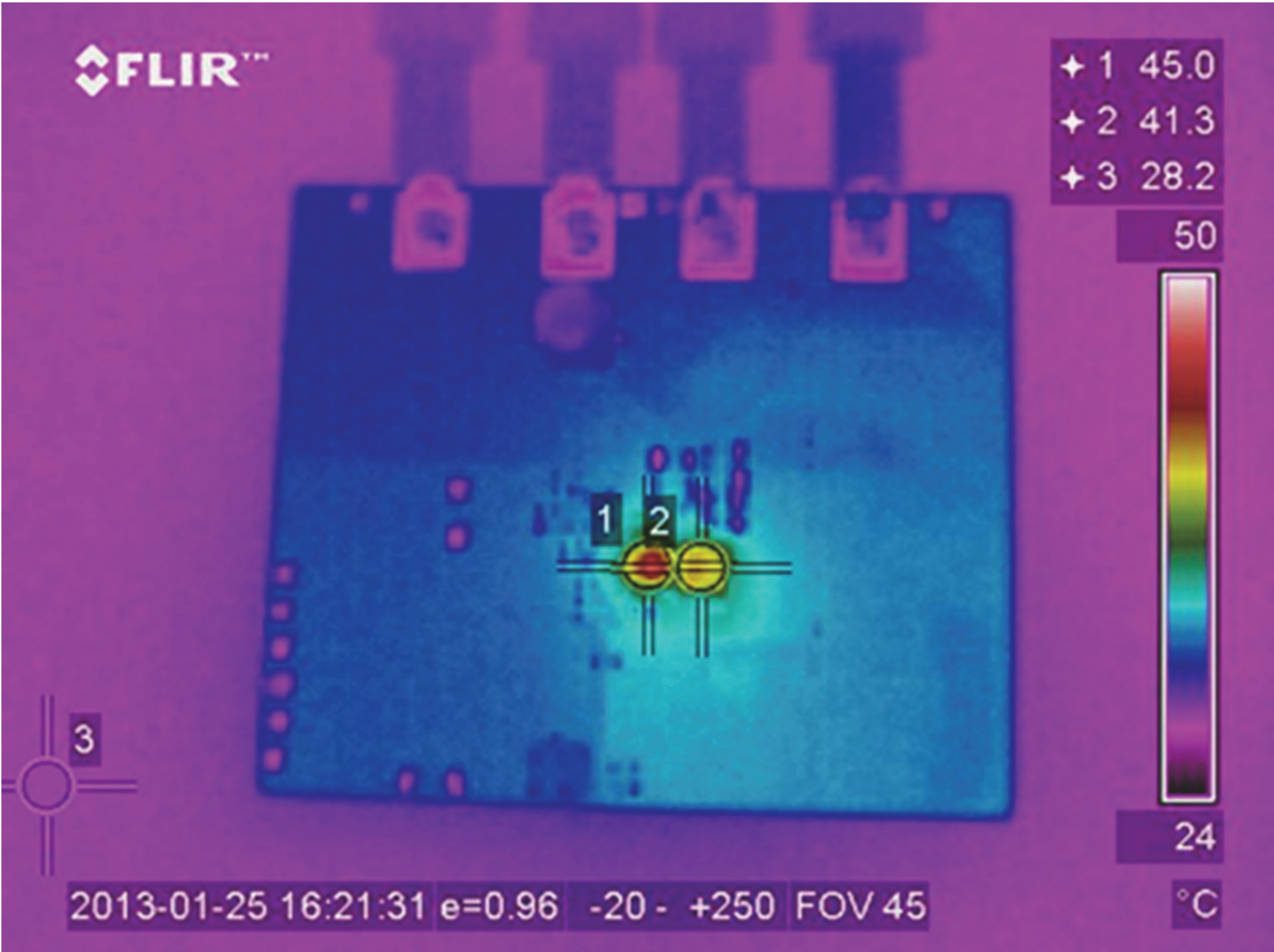


Fig. 19: Thermal Image of the board at 3A load
Test point 1 is IR3823
Test point 2 is inductor

PCB METAL AND COMPONENT PLACEMENT

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes. For further information, please refer to “SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note**.” (AN1132)**

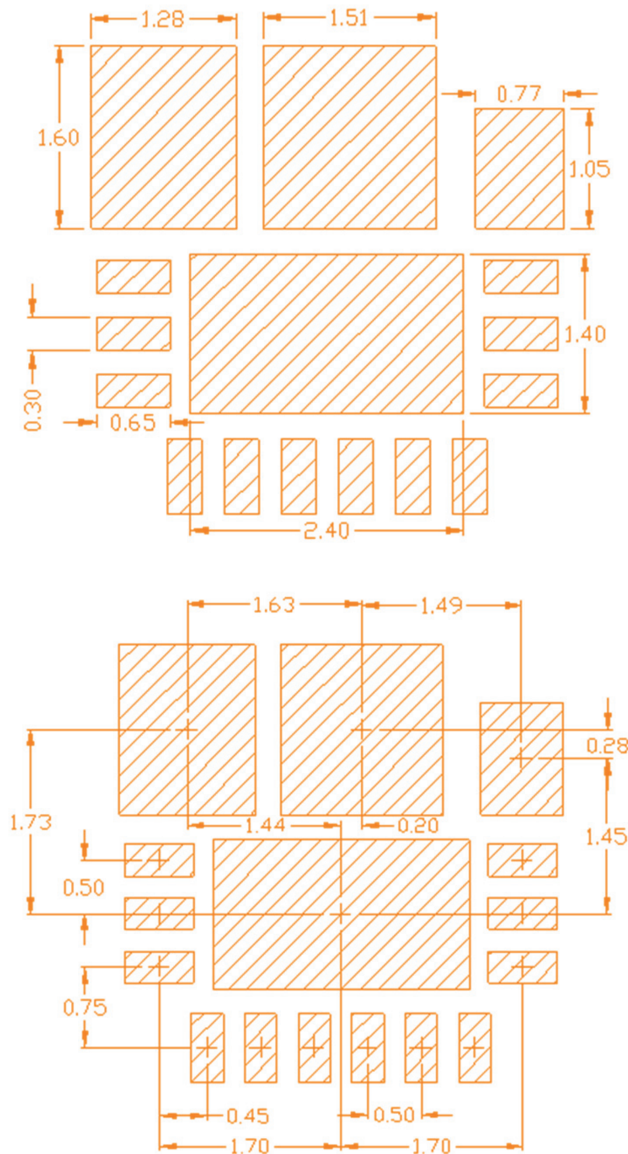


Figure 20: PCB Metal Pad Spacing (all dimensions in mm)

SOLDER RESIST

IR recommends that the larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying Copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1mm in X & Y.) However, for the smaller signal type leads around the edge of the device, IR recommends that these are Non Solder Mask Defined or Copper Defined. When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025mm on each edge, (i.e. 0.05mm in X&Y,) in order to accommodate any layer to layer misalignment. Ensure that the solder resist in-between the smaller signal lead areas are at least 0.15mm wide, due to the high x/y aspect ratio of the solder mask strip.

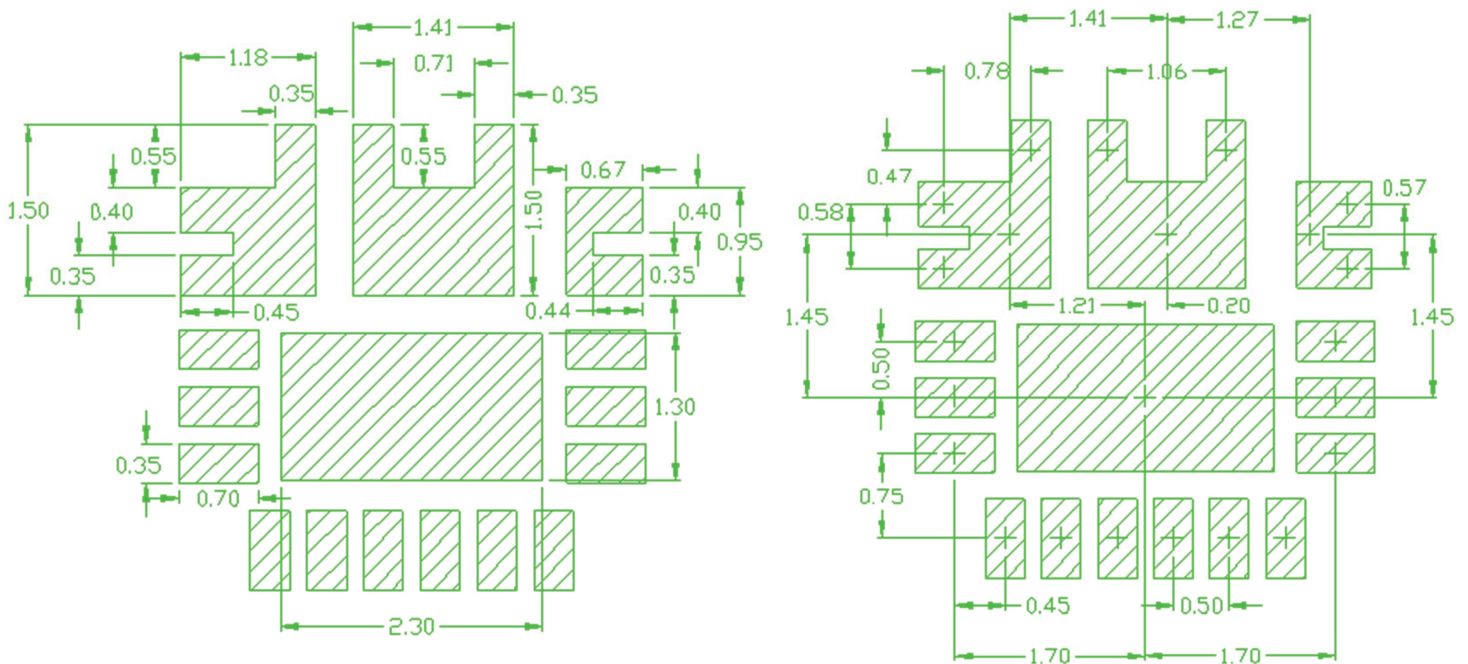


Figure 21: Solder Resist (all dimensions in mm)

STENCIL DESIGN

Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results. Evaluations have shown that the best overall performance is achieved using the stencil design shown in following figure. This design is for a stencil thickness of 0.127mm (0.005").The reduction should be adjusted for stencils of other thicknesses.

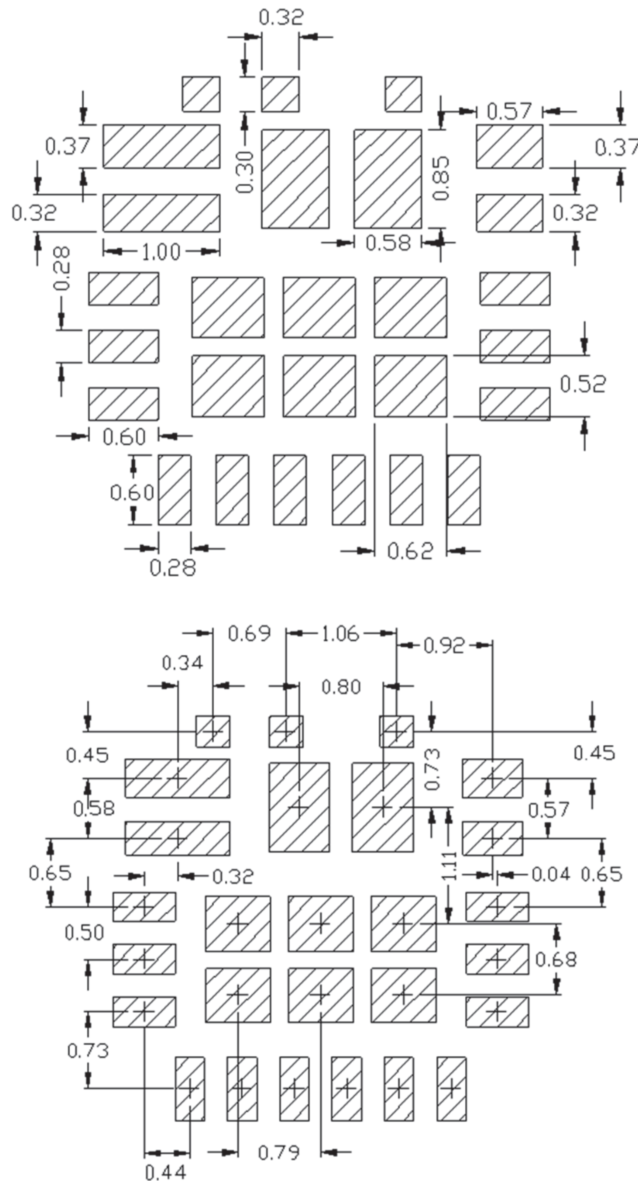
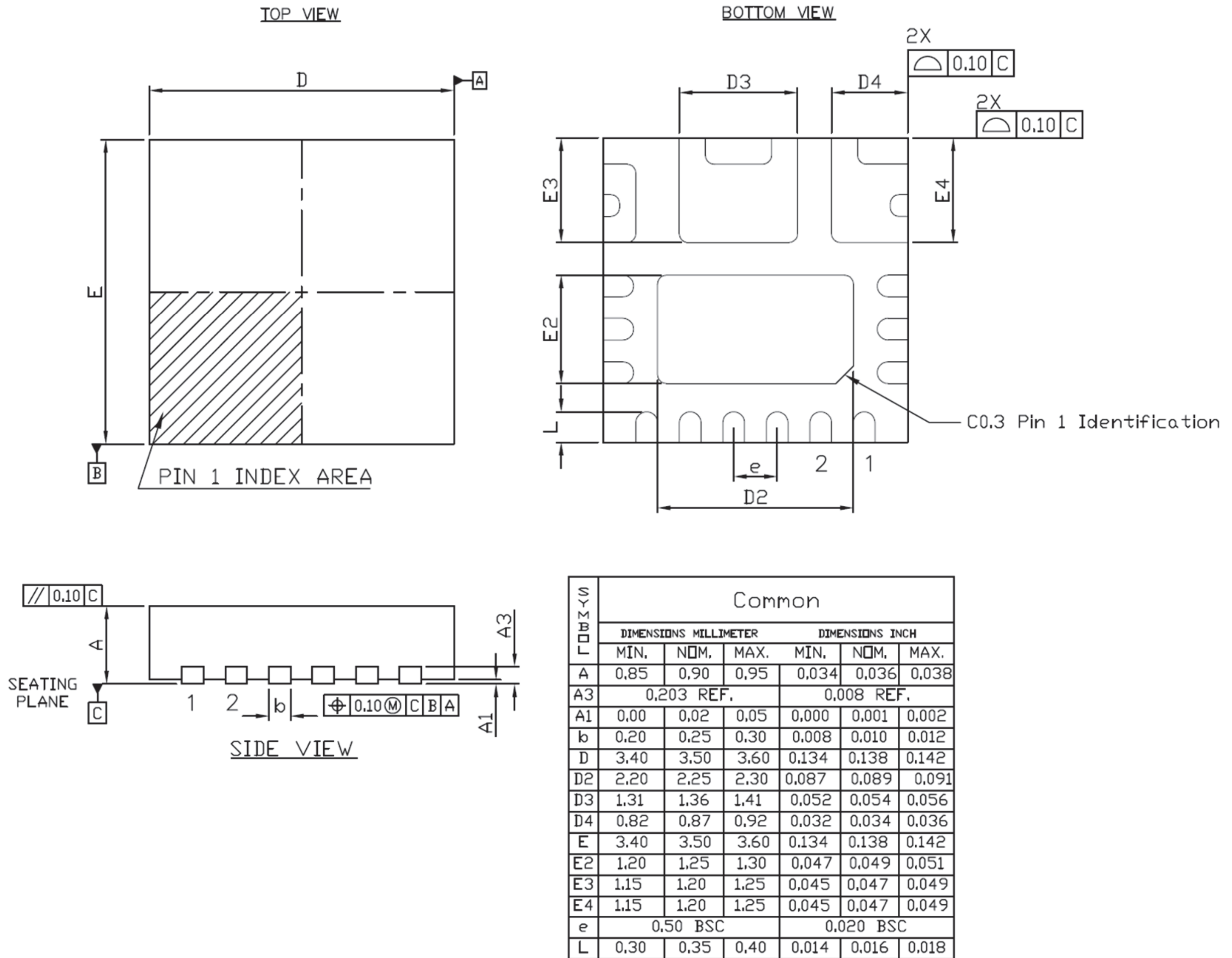


Figure 22: Stencil Pad Spacing (all dimensions in mm)

PACKAGE INFORMATION



SYMBOL	Common					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.034	0.036	0.038
A3	0.203 REF.			0.008 REF.		
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.40	3.50	3.60	0.134	0.138	0.142
D2	2.20	2.25	2.30	0.087	0.089	0.091
D3	1.31	1.36	1.41	0.052	0.054	0.056
D4	0.82	0.87	0.92	0.032	0.034	0.036
E	3.40	3.50	3.60	0.134	0.138	0.142
E2	1.20	1.25	1.30	0.047	0.049	0.051
E3	1.15	1.20	1.25	0.045	0.047	0.049
E4	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.30	0.35	0.40	0.014	0.016	0.018

Figure 23: Package Dimensions

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This product has been designed and qualified for the Industrial market

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Data and specifications subject to change without notice.